In the Specification:

Please replace paragraph [00004] beginning at page 2, with the following rewritten paragraph:

[00004] The upper NFET device (UFET) 3 is turned on and off by an upper gate-switching signal UGATE applied to its gate from driver 2, while the lower NFET device (LFET) 4 is turned on and off by a lower gate-switching signal LGATE supplied from driver 2. A common or phase node 5 between the two NFETs is coupled through an inductor 6 to a load reservoir capacitor 7 that is coupled to a reference voltage terminal (GND). The connection 8 between inductor 6 and capacitor 7 serves as an output node from which a desired (regulated) DC output voltage Vout is applied to a LOAD 9 (coupled to GND).

Please replace paragraph [00005] beginning at page 3, with the following rewritten paragraph:

[00005] The output node connection 8 is also fed back via a feedback resistor ~~10~~ 12 to error amplifier circuitry within the PWM controller 1. The error amplifier circuitry is used to regulate the converter's DC output voltage relative to a reference voltage supply. In addition, the common node 5 between the controllably switched NFETs is coupled via a current sense resistor 11 to current-sensing circuitry within the controller 1, in response to which the controller adjusts duty ratio of the PWM signal, as necessary, to maintain the converter's DC output within a prescribed set of parameters.